REMARKS

Claims 1-5, 21 and 22 are pending in this case. Claims 1, 3-5, 21 and 22 are amended with this response. Reconsideration of the application in light of the following remarks is respectfully requested.

I. REJECTION OF CLAIMS 1-5, 21 and 22 UNDER 35 U.S.C. § 103(a)

Claims 1-5, 21 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Moise et al. U.S. Patent No. 6,211,035 (Moise) in view of Fox et al. U.S. Patent No. 6,627,930 (Fox).

Claims 1-5 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Uchiyama et al. US Patent No. 6,831, 313 (Uchiyama) in view of Fox et al. U.S. Patent No. 6,627,930 (Fox). Withdrawal of the rejection is respectfully requested for at least the following reasons.

Claim 1 has been amended to recite *an integrated circuit, comprising an array of ferroelectric memory cells, each cell having a capacitor stack having an upper electrode, a lower electrode,* ***a lower conductive barrier layer underlying the lower electrode,*** *and a single ferroelectric core layer disposed between the upper and lower electrodes, wherein the single ferroelectric core layer comprises a crystallization in the (001) family, wherein at least 40% of the domains of the single ferroelectric core layer are functionally oriented with respect to the capacitor stack. The integrated circuit further comprises a conductive contact formed under at least one of the capacitor stacks, wherein* ***the conductive contact has a cross section at a contact portion that contacts a bottom portion of the capacitor stack that is about as large or larger than that of the ferroelectric core layer****.*

Applicant respectfully submits that amended independent claim 1 is patentable over Moise in view of Fox as the references do not teach or suggest a ferroelectric memory cell of an integrated circuit having a capacitor stack having (in one non-limiting example) an upper electrode (*e.g.*, 124), a lower electrode (*e.g.*, 120), **a lower conductive barrier layer** (in one non-limiting example, 118) **underlying the lower electrode** (*e.g.*, 120), and a single ferroelectric core layer (*e.g.*, 122) disposed between

the upper and lower electrodes, wherein a conductive contact (*e.g.*, 114) formed under the capacitor stack (*e.g.*, 125) has a cross section **at a contact portion** that contacts a bottom portion of the **capacitor stack** (*e.g.*, 125) **that is about as large or larger than that of the ferroelectric core layer** (*e.g.*, 122).

Although, the office (in OA dated June 13, 2008, page 11, par. 4 to page 12) points to Figs. 6a-6c and considers TiAlN layer 604 as the conductive contact and PZT layer 608 as the ferroelectric core layer, Moise identifies the TiAlN layer 604 as a **bottom conducting diffusion barrier layer 604** (col. 9, ll. 7-8), which would therefore clearly be more consistent with the **lower conductive barrier layer** (in one non-limiting example, item 118 of Fig. 4) as recited in claim 1 as well as claim 22, which therefore leaves the **lower contact plug as item 320** of Figs. 6c and 6f of Moise, or **2nd conductive contact 1020** of Figs. 10b and 10d Moise. Thus, lower contact plugs 320 of 6c and 6f or 1020 of Figs. 10b and 10d of Moise appear to be clearly **smaller than** that of the ferroelectric capacitor core PZT layer 608 of Moise. Furthermore, this size distinction between the recited conductive contacts and the Ferroelectric core layer is not trivial, because, for example, the larger conductive contacts provide compressive forces, which adds to the thermal stresses during cooling that reorient the domains within the Ferroelectric core, thereby aiding in the desired formation of the PZT crystal polarization recited in claims 1 and 22. (See *e.g.*, generally on Pg. 5, ll. 12-19, 22-27, and more particularly regarding the lower contact 114 on Pg. 11, ll. 13-21, and regarding the upper conductive contact 136 on Pg. 15, ll. 26-29 of the applicants invention).

The same discussions and conclusion also applies to Uchiyama. Although Uchiyama has a conductive **diffusion barrier layer 121** (col. 9, ll. 44) and a **lower conductive contact/plug 120** (col. 9, ll. 40-41), plug 120 does not have a cross-section near a contact portion with the bottom portion of the capacitor stack 128 that is about as large or larger than that of the ferroelectric cores 124. This is because the contact portion of Uchiyama (as defined by the capacitor stack layers recited in claim 1) would be between the diffusion barrier layer 121 and plug 120 of Uchiyama.

Here again, according to one non-limiting aspect of the present invention, the metal plugs filling the vias in the dielectric layer under (and/or over) the ferroelectric cores must, as recited in claim 1, be equal to or greater than that of the ferroelectric cores in order to sufficiently add to the thermal stresses that help reorient the domains during cooling (See *e.g.*, page 5 lines 24-27 and page 7 lines 7-11 of the applicants invention). Fox is not applied to teach the underlying conductive contact. Accordingly, Applicant respectfully submits that claim 1 and the claims that depend therefrom are patentable over the references.

Claims 1, 3-5 and 21 were also amended to provide additional clarity regarding the ferroelectric core layer.

Claim 22 has been amended to recite *an integrated circuit, comprising an array of ferroelectric memory cells, each cell having a capacitor stack comprising* ***a lower conductive barrier layer, a lower electrode over the barrier layer, a single ferroelectric core layer*** *disposed between the upper and lower electrodes, wherein the single ferroelectric core layer comprises crystallization in the (001) family, wherein at least 40% of the domains of the single ferroelectric core layer are functionally oriented with respect to the capacitor stack,* ***an upper electrode over the single ferroelectric core layer, and an upper barrier over the upper electrode. The integrated circuit further comprises a first conductive contact formed over the capacitor stack****, and* ***a second conductive contact formed under the capacitor stack****. The* ***first and second conductive contacts each have a cross section at a contact portion of the capacitor stack that is about as large or larger than that of the ferroelectric core layer.***

Similar to the argument above for claim 1, the applicant respectfully submits that amended independent claim 22 is patentable over Moise in view of Fox as the references do not teach or suggest an integrated circuit comprising capacitor stacks each having an upper electrode, a lower electrode, and a single ferroelectric core layer, wherein the integrated further comprises ***a first conductive contact formed over the capacitor stack****, and* ***a second conductive contact formed under the capacitor stack*** wherein both *the* ***first and second conductive contacts each have a cross***

section at a contact portion of the capacitor stack that is about as large or larger than that of the ferroelectric core layer.

Again, by contrast, Moise identifies the TiAlN layer 604 as a **bottom conducting diffusion barrier layer 604** (col. 9, ll. 7-8), which would therefore clearly be more consistent with the **lower conductive barrier layer** (in one non-limiting example, item 118 of Fig. 4) as recited in claim 22, which therefore leaves the **lower contact plug as item 320** of Figs. 6c and 6f of Moise, or **2nd conductive contact 1020** of Figs. 10b and 10d Moise. Thus, lower contact plugs 320 of 6c and 6f or 1020 of Figs. 10b and 10d of Moise appear to be clearly **smaller than** that of the ferroelectric capacitor core PZT layer 608 of Moise.

The same discussion and conclusion also applies to Uchiyama, which has a contact 120 that does not have a cross-section near a contact portion with the bottom portion of the capacitor stack 128 that is about as large or larger than that of the ferroelectric cores 124. This is because the contact portion of Uchiyama (as defined by the layers of the capacitor stack recited in claim 22) would be between the diffusion barrier layer 121 and plug 120 of Uchiyama. According to one non-limiting aspect of the present invention, the **larger upper and lower conductive contacts** provide compressive forces, which adds to the thermal stresses during cooling that reorient the domains within the Ferroelectric core, thereby aiding in the desired formation of the PZT crystal polarization recited in claims 1 and 22. (See *e.g.*, generally on Pg. 5, ll. 12-19, 22-27, and more particularly regarding the lower contact 114 on Pg. 11, ll. 13-21, and regarding the upper conductive contact 136 on Pg. 15, ll. 26-29 of the applicants invention). Again, Fox is not applied to teach the upper and lower conductive contacts. Accordingly, Applicant respectfully submits that claim 22 is patentable over the references.

In addition, Fox et al. do not teach a **single ferroelectric core layer,** as recited in claims 1 and 22. By contrast, Fox et al. teach **a multi-layered** crystallographic textured structure, wherein the multiple "textures" describe multiple "crystal planes" (column 1, lines 60-61 of Fox et al.) of multiple ferroelectric layers, or a *first ferroelectric layer having a first crystallographic texture and a second ferroelectric layer having a*

second differing crystallographic texture (Abstract, lines 6-10 of Fox et al.), and therefore the cited art does not teach this feature of the claimed invention.

In addition, Fox et al. teach against the **single ferroelectric core layer** structure of claims 1 and 22 of the present invention, for example, stating that *the **multi-layered ferroelectric capacitors** disclosed provide much enhanced performance and operating characteristics over conventional ferroelectric devices incorporating dielectric layers having **but a single crystallographic texture*** (a single Fe-layer) (Column 2, lines 59-63 of Fox et al.). Thus, one would not be motivated to combine the teaching of Fox et al. teaching ***multiple ferroelectric layers*** with Uchiyama et al. teaching a ***single homogenous ferroelectric core*** (Column 2, lines 18-22 of Uchiyama et al.) because such a modification would render the structure of Fox et al. unsatisfactory for it's intended purpose.

Fox et al. also teach against the **single ferroelectric core layer** structure of claims 1 and 22 of the present invention, for example, teaching that *the **use of the added ferroelectric layer 24*** significantly reduces the undesired effects of dipole "pinning" which might otherwise occur when the bottom or top electrodes 12, 14 directly adjoin the ferroelectric bulk (core) (Column 2, lines 37-40 of Fox et al.). Thus, one would not be motivated to combine the above teachings of Fox et al. with Uchiyama et al. teaching a ***single homogenous ferroelectric core** material*, or a ***single composite material** comprising a ferroelectric component and a dielectric component* (Abstract, lines 3-6, and Column 2, lines 18-22 of Uchiyama et al.)

Finally, Fox et al. discourage the <001> ***crystallization family*** orientation recited in claims 1 and 22, stating that growing ***ferroelectric dielectric layers having a <001> crystallographic texture*** *is generally **more difficult than growing** <111> or RND material,* which *is generally utilized* (Column 4, lines 17-21 of Fox et al.).

As highlighted above, the primary reference, Moise et al., do not teach the invention of independent claims 1 or 22, and one of ordinary skill in the art would not be motivated to combine with Fox et al. or be motivated to modify the reference in accordance with Uchiyama et al. Therefore claims 1-5, 21 and 22 are believed to be

non-obvious over the cited art, and withdrawal of the rejections is therefore respectfully requested.

III. CONCLUSION

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 20-0668, TI-36398.

Respectfully submitted,
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